

SoC Verification Engineer

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Phone :

Web :



Job Summary

Vacancy :

Deadline : Jan 01, 1970

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Employment Status : Full Time

Experience : 3 - <5 Years

Salary :

Gender : Any

Career Level : Any

Qualification : B.Tech

Job Description

Experience: 4–10 Years

Contract Type: Subcontract

Start Date: Immediate to 3 Weeks

Location:

We are looking for experienced SoC Verification Engineers with strong hands-on expertise in SystemVerilog / UVM and solid understanding of SoC protocols and verification methodologies.

Key Responsibilities:

- Strong hands-on experience with SV / UVM
- Good understanding of AXI4, PCIe, Ethernet, NoC, UCIe
- Experience in testbench development & UVM test case coding
- Solid understanding of coverage closure
- Knowledge of encryption & decryption is a plus

Education & Experience

Must Have

Educational Requirements

B.Tech

Compensation & Other Benefits
